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Title	NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING THE SAME

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APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

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1. ■ Fee Transmittal Form (e.g. PTO/SB/17)
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2. ■ Specification Total Pages **38**

3. ■ Drawing(s) *(35 U.S.C. 113)* Total Sheets **13 (Formals)**

4. □ Oath or Declaration Total Pages
   a. □ Newly executed (original or copy)
   b. □ Copy from a prior application *(37 C.F.R. §1.63(d))*
   (for continuation/divisional with box 15 completed)
      i. □ DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see *37 C.F.R. §1.63(d)(2) and 1.33(b).*

5. □ Incorporation By Reference *(usable if box 4B is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4B, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

ACCOMPANYING APPLICATION PARTS

6. □ Assignment Papers (cover sheet & document(s))
7. □ 37 C.F.R. §3.73(b) Statement *(when there is an assignee)* □ Power of Attorney
8. □ English Translation Document *(if applicable)*
9. ■ Information Disclosure Statement (IDS)/PTO-1449 ■ Copies of IDS Citations (1)
10. □ Preliminary Amendment
11. ■ White Advance Serial No. Postcard
12. □ Small Entity Statement(s) □ Statement filed in prior application. Status still proper and desired.
13. ■ Certified Copy of Priority Document(s) (1)
(if foreign priority is claimed)
14. ■ Other: Notice of Priority, List of Inventors' Names and Addresses

15. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below:*
□ Continuation □ Divisional □ Continuation-in-part (CIP) of prior application no.:
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16. Amend the specification by inserting before the first line the sentence:
□ This application is a □ Continuation □ Division □ Continuation-in-part (CIP)
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□ This application claims priority of provisional application Serial No. Filed

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TITLE OF THE INVENTION

NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 11-118115, filed April 26, 1999, the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

This invention relates to a nonvolatile semiconductor memory device and a method for manufacturing the same.

As is well known in the art, a semiconductor memory has cell transistors and peripheral transistors formed on the same substrate. As one example thereof, an electrically erasable and programmable read only memory in which data erasing and programming can be electrically effected is well known.

FIG. 1 shows an EEPROM. That is, FIG. 1 schematically shows the construction of cell transistors (including selection gate transistors) and peripheral transistors of a conventional NAND type EEPROM.

The construction of the cell transistor and peripheral transistor of the NAND type EEPROM is explained below according to the manufacturing process

thereof.

FIGS. 2A to 2D show the manufacturing process of the cell transistors and peripheral transistors of the conventional NAND type EEPROM.

First, as shown in FIG. 2A, for example, after a well region and element isolation region (neither of them is shown in the drawing) are formed in the surface area of a silicon substrate 101, a thermal oxidation film 102 used as a gate insulating film or tunnel oxide film is formed on the well region.

Then, in the memory cell region, gate electrodes 103 of stacked gate structure are formed on the thermal oxidation film (tunnel oxide film) 102 and, in the peripheral circuit region, gate electrodes 104 of single-layered structure are formed on the thermal oxide film (gate insulating film) 102.

The gate electrode 103 in the memory cell region has a well known structure in which, for example, a control gate electrode 103c is stacked on a floating gate 103a used as a charge storing layer while an ONO film (oxide film/nitride film/oxide film) 103b used as an inter-gate insulating film is disposed therebetween.

Next, as shown in FIG. 2B, post-oxidation films 105 for restoring the gate electrodes 103, 104 from the processing damage are formed.

Then, as shown in FIG. 2C, impurity 106 is implanted to form source and drain diffusion regions of

the respective transistors.

After this, as shown in FIG. 2D, the implanted impurity 106 is activated by annealing and driven towards the channel region side to form source and drain diffusion layers 106'.

Next, after an inter-level insulating film 107 is formed on the structure, contacts 108 and inter-connection layers 109 connected to the electrodes 104 and contacts 110 and bit lines 111 connected to the source/drain diffusion layers 106' are formed to form the cell transistors and peripheral transistors of the structure shown in FIG. 1.

However, if the conventional cell transistors and peripheral transistors are formed as described above, the length of the overlap area of the source/drain diffusion layer 106' over the gate electrode 103 or 104 varies depending on the condition of the annealing process effected after the impurity 106 is implanted.

For example, if the annealing process is not sufficiently effected and the source/drain diffusion layer 106' does not overlap and is offset from the gate electrode 103 or 104, the offset portion acts as a parasitic resistor to prevent a sufficiently large drain current from flowing in the device.

On the other hand, if the annealing process is excessively effected and the source/drain diffusion layer 106' extends deeply into the channel region, the

short channel effect becomes significant and the source-drain withstand voltage is lowered, thereby degrading the device characteristic.

Generally, the gate length in the memory cell is shorter than that in the peripheral transistor. Therefore, the short channel effect in the memory cell tends to become more noticeable. That is, if the annealing process is sufficiently effected for the peripheral transistor, there occurs a possibility that punch through may occur in the cell transistor and selection transistor.

In the case of NAND type EEPROM, since the source and drain diffusion layers 106' of the memory cells are satisfactory if they can electrically connect the cells which are serially arranged, it is not necessary to overlap the source/drain diffusion layer 106' over the gate electrode 103. That is, it can be the that the annealing process after the impurity 106 is implanted is effected to the least possible degree from the viewpoint of the characteristic of the cell transistor and selection transistor.

Further, in the case of the post-oxidation amount after the gate processing, the post-oxidation for sufficiently compensating for the processing damage is necessary, but the post-oxidation increases the bird's beak amount. In a case where the memory cell has a short gate, an increase in the bird' beak amount by the

post-oxidation (refer to a portion A in FIG. 1, for example) lowers the coupling ratio, degrades the programming and erasing characteristics and is not preferable.

In the case of the peripheral transistor, since the gate is relatively long, it is permitted to sufficiently effect the post-oxidation (refer to a portion B in FIG. 1, for example).

Thus, since the NAND type EEPROM includes transistors having different gate lengths and the post-oxidation amount and the most suitable annealing condition for impurity diffusion are different depending on the gate lengths of the transistors, the difference causes a main factor which lowers the process margin.

BRIEF SUMMARY OF THE INVENTION

A first object of this invention is to provide a nonvolatile semiconductor memory device in which the annealing condition for diffusion of impurity and post-oxidation amount can be controlled according to the gate lengths of transistors to attain the high performance of the device and a method for manufacturing the same.

A second object of this invention is to provide a nonvolatile semiconductor memory device in which an amount of electrons trapped into the gate insulating film can be reduced and a method for manufacturing the

same.

In order to attain the first object, a nonvolatile semiconductor memory device according to one aspect of this invention comprises a semiconductor substrate, a first transistor formed in a peripheral circuit portion of the semiconductor substrate, a gate electrode of the first transistor having a first gate length, a second transistor formed in a memory cell portion of the semiconductor substrate, a gate electrode of the second transistor having a second gate length shorter than the first gate length, and a first insulating film formed above at least the memory cell portion, the first insulating film covering the second transistor and having a property which makes it difficult for an oxidizing agent to pass therethrough.

The above nonvolatile semiconductor memory device has the first insulating film selectively formed above the memory cell portion. The first insulating film covers the second transistors and has a property which makes it difficult for oxygen to pass therethrough. Therefore, in the memory cell portion in which the second transistors are formed, oxidation thereof can be suppressed and in the peripheral circuit portion in which the first transistors are formed, oxidation thereof can be activated.

Thus, by making the oxidation amount of the memory cell portion different from the oxidation amount of the

peripheral circuit portion, the annealing condition for diffusion of impurity and post-oxidation amount for the first and second transistors can be controlled to an optimum state even if the gate length of the second transistor is smaller than the gate length of the first transistor. Therefore, the high performance of the device can be attained.

In order to attain the second object, a nonvolatile semiconductor memory device according to another aspect of this invention comprises a semiconductor substrate, a transistor formed in a memory cell portion of the semiconductor substrate, and a silicon nitride film whose surface is oxidized, the silicon nitride film covers the transistor.

The above nonvolatile semiconductor memory device has the silicon nitride film having the surface thereof oxidized. In comparison with a silicon nitride film whose surface is not oxidized, in the silicon nitride film having the surface thereof oxidized, the concentration of hydrogen contained in the film is reduced. Therefore, if the transistors formed in the memory cell portion are covered with the silicon nitride film, an amount of hydrogen moving towards the transistors can be reduced. As a result, for example, it is possible to reduce the amount of hydrogen entrapped into the gate insulating film of the transistor.

Since the gate insulating film in which an amount of entrapped hydrogen is small can be obtained, an amount of electrons which are trapped into the gate insulating film each time the electrons move in the gate insulating film can be reduced. Therefore, it is possible to reduce the amount of electrons trapped into the gate insulating film.

Additional objects and advantages of the invention will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The objects and advantages of the invention may be realized and obtained by means of the instrumentalities and combinations particularly pointed out hereinafter.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate presently preferred embodiments of the invention, and together with the general description given above and the detailed description of the preferred embodiments given below, serve to explain the principles of the invention.

FIG. 1 is a cross sectional view showing a conventional NAND type EEPROM;

FIGS. 2A, 2B, 2C and 2D are cross sectional views showing the conventional NAND type EEPROM in the respective main manufacturing steps;

FIG. 3A is a plan view showing a NAND type EEPROM according to a first embodiment of this invention;

FIG. 3B is a cross sectional view taken along the 3B-3B line of FIG. 3A;

FIG. 4 is a circuit diagram showing an equivalent circuit of the NAND type EEPROM;

FIGS. 5A, 5B, 5C and 5D are cross sectional views showing the NAND type EEPROM according to the first embodiment of this invention in the respective main manufacturing steps;

FIG. 6 is a cross sectional view showing a first modification of the NAND type EEPROM according to the first embodiment of this invention;

FIG. 7 is a cross sectional view showing a second modification of the NAND type EEPROM according to the first embodiment of this invention;

FIG. 8 is a cross sectional view showing a third modification of the NAND type EEPROM according to the first embodiment of this invention;

FIGS. 9A and 9B are cross sectional views each showing one example of formation of a contact hole;

FIGS. 10A and 10B are cross sectional views each showing another example of formation of a contact hole;

FIG. 11 is a plan view showing a fourth modification of the NAND type EEPROM according to the first embodiment of this invention;

FIG. 12 is a cross sectional view showing a fifth

modification of the NAND type EEPROM according to the first embodiment of this invention;

FIG. 13 is a cross sectional view showing a NAND type EEPROM according to a second embodiment of this invention;

FIGS. 14A, 14B, 14C and 14D are cross sectional views showing the NAND type EEPROM according to the second embodiment of this invention in the respective main manufacturing steps;

FIG. 15 is a diagram showing the characteristic of the NAND type EEPROM according to the second embodiment of this invention in comparison with the characteristic of the conventional NAND type EEPROM;

FIG. 16A is a circuit diagram showing an equivalent circuit of an AND type EEPROM; and

FIG. 16B is a circuit diagram showing an equivalent circuit of a NOR type EEPROM.

DETAILED DESCRIPTION OF THE INVENTION

There will now be described embodiments of this invention with reference to the accompanying drawings. In the present embodiments, for example, a NAND type EEPROM is used as a nonvolatile semiconductor memory device.

(First Embodiment)

FIG. 3A is a plan view showing the schematic construction of a NAND type EEPROM according to a first embodiment of this invention and FIG. 3B is a cross

sectional view taken along the 3B-3B line of FIG. 3A.

As shown in FIGS. 3A, 3B, the NAND type EEPROM has a memory cell region (cell array) 12 and peripheral circuit region 13 formed on a silicon substrate 11, for example.

In the memory cell region 12, memory cell transistors, selection gate transistors and the like are formed. In this embodiment, transistors formed in the memory cell region 12 are generally called cell transistors.

Further, in the peripheral circuit region 13, transistors constituting a memory core circuit including a row decoder, column decoder, sense amplifiers and the like and transistors constituting an I/O circuit are formed. In this embodiment, transistors formed in the peripheral circuit region 13 are generally called peripheral transistors.

An element isolation region 12b is formed on the surface of the silicon substrate 11 in the memory cell region 12. The element isolation regions 12b separate a plurality of stripe-form element regions 12a formed in the memory cell region 12 and extending in the column direction. In the element regions 12a, for example, the surface of a p-type well region formed on the silicon substrate 11 is exposed.

In part of the element regions 12a, n-type source diffusion layers 21a are formed, and in another part of

the element regions 12a, n-type drain diffusion layers 21b are formed. Between the source diffusion layer 21a and the drain diffusion layer 21b, eighteen cell transistors are formed. The eighteen cell transistors are serially connected.

The cell transistor among the eighteen cell transistors which is connected to the source diffusion layer 21a is a source side selection gate transistor SGS and the cell transistor connected to the drain diffusion layer 21b is a drain side selection gate transistor SGD. The remaining sixteen cell transistors except the above two cell transistors are memory cell transistors ST. The sixteen memory cell transistors ST serially connected to one another constitute one unit cell (NAND cell).

Each of the memory cell transistors ST includes a gate oxide film 31, gate electrode 35 and source and drain diffusion layers 21 formed in the element region 12a.

The gate electrode 35 of the memory cell transistor ST of this example has a stacked gate structure. The stacked gate structure is constructed by a floating gate 32 formed on the gate oxide film 31, an inter-gate insulating film 33 formed on the floating gate 32, and a control gate 34 formed on the inter-gate insulating film 33. For example, the gate oxide film 31 is formed by oxidizing the surface of the substrate

11 which is exposed in the element region 12a. In a NAND type EEPROM using a tunnel current at the data programming/erasing, the gate oxide film 31 is also called a tunnel oxide film. The floating gate 32 stores charges (generally, electrons) to control the threshold voltage of the memory cell transistor ST and is also called a charge storage layer. The inter-gate insulating film 33 isolates the floating gate 32 and control gate 34 from each other and is formed of a silicon oxide film/silicon nitride film/silicon oxide film (ONO film), for example. The control gates 34 on the same row are connected to a corresponding one of word lines WL0 to WL15 for selecting the row of the cell array.

The drain side selection gate transistor SGD of this example has substantially the same structure as the memory cell transistor ST except that one of the source and drain diffusion layers 21 is formed of the drain diffusion layer 21b.

Likewise, the source side selection gate transistor SGS of this example has substantially the same structure as the memory cell transistor ST except that one of the source and drain diffusion layers 21 is formed of the source diffusion layer 21a.

The outer surface of the gate electrode 35 is covered with a first insulating film 37 formed of a silicon nitride (SiN) film with a post-oxidation film

36 disposed therebetween. That is, the first insulating film 37 is selectively formed only on the memory cell region 12 so as to cover all of the cell transistors ST, SGS, SGD.

An inter-level insulating film 38 is formed on the first insulating film 37. In the inter-level insulating film 38, contacts 39b and 39a passing through a thermal oxide film (in this example, which is formed of the same thermal oxide film as the gate oxide film 31) formed on the element regions 12a and the first insulating film 37 and respectively reaching the drain diffusion layers 21b and source diffusion layers 21a are formed.

On the inter-level insulating film 38, bit lines (BL1, BL2, ···) 40 connected to the drain diffusion layers 21b via the contacts 39b are formed in the column direction. In the inter-level insulating film 38, source lines (SL) connected to the source diffusion layers 21a via the contacts 39a are formed in a row direction perpendicular to the column direction. Thus, a memory cell array of the NAND type EEPROM shown in FIG. 4 is constructed.

As shown in FIG. 3B, each of the peripheral transistors CT formed in the peripheral circuit region 13 includes a gate oxide film 31, gate electrode 41 and source/drain diffusion layers 42, 43.

The gate electrode 41 of the peripheral transistor

CT of this example has a gate length larger than that of the gate electrode 35 of the cell transistors ST, SGD, SGS. The structure thereof is not the stacked gate structure but is a general gate structure having a single-layered gate electrode. The general gate structure is hereinafter referred to as a single-gate structure for convenience in this specification.

Further, the outer surface of the gate electrode 41 is covered with only a post-oxidation film 36.

An inter-level insulating film 38 is formed on the post-oxidation film 36. Contacts 44 each passing through the post-oxidation film 36 and reaching the gate electrode 41 are formed in the inter-level insulating film 38.

Interconnection layers 45 each connected to a corresponding one of the gate electrodes 41 via the contact 44 are formed on the inter-level insulating film 38.

Next, one example of a manufacturing method of the NAND type EEPROM according to the first embodiment is explained.

FIGS. 5A, 5B, 5C and 5D are cross sectional views showing the NAND type EEPROM according to the first embodiment of this invention in the respective main manufacturing steps.

First, as shown in FIG. 5A, an element isolation region 12b is formed on the surface of a silicon

substrate 11 to isolate element regions 12a. Since the cross section of FIG. 5A is taken along the element region 12a, the element isolation region 12b is not shown in FIG. 5A. Then, a portion of the substrate 11 (or well region) exposed in the element region 12a is subjected to the thermal oxidation process to form a thermal oxidation film. The thermal oxidation film is used as a gate insulating film 31. Next, gate electrodes 35 of stacked gate structure are formed on the gate oxide film 31 in the memory cell region 12 and gate electrodes 41 of single-gate structure are formed on the gate oxide film 31 in the peripheral circuit region 13. The above gate electrodes are both formed to cross the element regions 12a, for example. The gate electrodes 35 of stacked gate structure can be formed by use of a well known method. As one example of the method, a method for forming a floating gate 32 on the gate oxide film 31, forming an inter-gate insulating film 33 on the floating gate 32 and forming a control gate 34 on the inter-gate insulating film 33 is given. After this, the surfaces of the gate electrodes 35, 41 are subjected to the oxidation process. The oxidation process is effected to compensate for the processing damage of the gate electrodes 35, 41. As a result, post-oxidation films 36 are formed on the surfaces of the gate electrodes 35, 41. Then, impurity 21' is ion-implanted into the

element regions 12a with the gate electrodes 35, 41 and element isolation region 12b used as a mask. The impurity 21' is ion-implanted to form diffusion layers 21, 21a, 21b, 42, 43 of transistors (ST, SGS, SGD, CT).

Next, as shown in FIG. 5B, a first insulating film 37 formed of a silicon nitride film is deposited on the structure shown in FIG. 5A. The first insulating film 37 is not limited to the silicon nitride film and a film which makes it difficult for an oxidizing agent (oxidizing seed) to pass therethrough at the later annealing time in an oxidation atmosphere may be used.

After this, as shown in FIG. 5C, the first insulating film 37 formed on the peripheral circuit region 13 is removed. When the above removing process is effected, a photoresist pattern covering the memory cell region 12 or a photoresist pattern having an window corresponding to the peripheral circuit region 13 is formed by use of the photolithography technology, for example. Then, the first insulating film 37 may be removed by effecting a CDE (Chemical Dry Etching) method using the above photoresist pattern as a mask.

Next, as shown in FIG. 5D, the doped impurity 21' is activated by annealing in the oxidation atmosphere. As a result, the doped impurity 21' is diffused in the depth direction of the substrate 11 and in the lateral direction towards a portion below each of the gate electrodes 35, 41. Thus, diffusion layers 21, 21a,

21b, 42, 43 are formed.

As described above, the structure having the memory cell region 12 covered with the first insulating film 37, that is, the structure shown in FIG. 5C is subjected to the annealing process in the oxidation atmosphere. At this time, since the first insulating film 37 is not formed on the surface of the peripheral circuit region 13, a larger amount of oxidizing agent reaches the silicon substrate 11 in the peripheral circuit region 13 than in the memory cell region 12. Therefore, the diffusion speed of the impurity 21' in the peripheral circuit region 13 is increased so that the source/drain diffusion layers 42, 43 will sufficiently overlap the gate electrode 41.

Since the memory cell region 12 is covered with the first insulating film 37, almost no oxidizing agent reaches the silicon substrate 11 in the memory cell region 12 even if the structure is subjected to the annealing process in the oxidation atmosphere. Therefore, the impurity 21' is not so diffused as in the peripheral transistor CT, thereby making it possible to suppress the short channel effect.

In a case where tungsten silicide (WSi) is used for the control gate 34, it is considered that abnormal oxidation of WSi will occur due to the annealing process effected in the oxidation atmosphere. The abnormal oxidation of WSi tends to occur in a portion

where the gate length of the cell transistor ST is small, for example.

However, in the first embodiment in which the memory cell region 12 is covered with the first insulating film 37, the abnormal oxidation of WSi can be suppressed even if WSi is used for the control gate 34 since the oxidizing agent can be suppressed from reaching the gate electrode 35.

Further, the bird' beak amount for the gate insulating film 31 in the memory cell region 12 and the post oxidation amount on the side wall of the gate electrode 35 can be reduced by leaving the first insulating film 37 on the memory cell region 12 in comparison with a case where the first insulating film 37 is removed. Reductions in the bird's beak amount and post oxidation amount are particularly effective for suppressing a lowering in the ratio (coupling ratio) of the capacitance between the control gate 34 and the floating gate 32 to the capacitance between the floating gate 32 and the substrate 11.

The post oxidation amount can be changed according to formation/non-formation of the first insulating film 37 for the peripheral transistor CT for which it is desired to sufficiently effect the post oxidation so as to compensate for the processing damage and for the cell transistors ST, SGS, SGD for which it is not desired to excessively effect the post oxidation.

Next, after an inter-level insulating film 38 is formed on the structure shown in FIG. 5D, contacts 44 and interconnection layers 45 connected to the gate electrodes 41 are formed, bit lines 40 and contacts 39b connected to the drain diffusion layers 21b are formed and source lines and contacts 39a connected to the source diffusion layers 21a are formed. As a result, a NAND type EEPROM of a structure shown in FIGS. 3A, 3B is completed.

In the first embodiment, the peripheral circuit region 13 can be selectively subjected to the oxidation process.

That is, the annealing process is effected in the oxidation atmosphere with the memory cell region 12 covered with the first insulating film 37. Therefore, even in a case where the gate lengths of transistors are different, it is possible to simultaneously satisfy the annealing condition for impurity diffusion and the post oxidation amount. As a result, reductions in the process margin due to a difference in the optimum annealing condition for impurity diffusion and the post oxidation amount depending on the gate lengths of the transistors can be suppressed and this invention is extremely useful for attaining the high performance of the device.

(First Modification of First Embodiment)

FIG. 6 is a cross sectional view showing a first

modification of the NAND type EEPROM according to the first embodiment of this invention.

As shown in FIG. 6, when the first insulating film 37 is removed, it is not necessary to remove the first insulating film for all of the peripheral transistors CT. That is, the first insulating film 37 may be removed only for the peripheral transistors CT in which it is desired to cause source/drain layers 42-1, 43-1 to sufficiently overlap a gate electrode 41-1 or the peripheral transistors CT in which it is desired to sufficiently effect the post-oxidation process.

(Second Modification of First Embodiment)

FIG. 7 is a cross sectional view showing a second modification of the NAND type EEPROM according to the first embodiment of this invention.

As shown in FIG. 7, like the structure of the gate electrode 35 of the cell transistor (ST, SGD, SGS), a gate electrode 41' of each of the peripheral transistors CT can be formed with a stacked gate structure. In this case, it is sufficient if the interconnection layer 45 is electrically connected to at least the first-layered gate electrode 32 as is well known in the art.

Further, in the second modification, an inter-gate insulating film 33 can be formed in the gate electrode 41' of the peripheral transistor CT. Therefore, the bird's beak amount for the inter-gate insulating film

33 can be made different in an area where the first insulating film 37 is left behind and in an area where it is removed.

(Third Modification of First Embodiment)

FIG. 8 is a cross sectional view showing a third modification of the NAND type EEPROM according to the first embodiment of this invention.

As shown in FIG. 8, a gate electrode 35' of the selection gate transistor SGD (SGS) can be formed with a structure different from the structure of the gate electrode 35 of the memory cell transistor ST.

In this example, the inter-gate insulating film 33 is removed from the gate electrode 35' of the selection gate transistor SGD.

A gate electrode 41'' of the peripheral transistor CT can also be formed with the same structure as the gate electrode 35' of the selection gate transistor SGD.

(Fourth Modification of First Embodiment)

FIGS. 9A and 9B are cross sectional views showing one example of formation of contact hole.

As shown in FIG. 9A, in the NAND type EEPROM according to this invention, the first insulating film 37 is formed on the element isolation region 12b and diffusion layer 21b. In this case, a material constituting the inter-level insulating film 38 and a material constituting the first insulating film 37 are

made different from each other. Further, as an etchant used for an RIE (Reactive Ion Etching) process for forming a contact hole 39b, an etchant which easily etches the inter-level insulating film 38 and is difficult to etch the first insulating film 37 is used. Thus, the etching process can be temporarily stopped at the first insulating film 37.

By thus temporarily stopping the etching process at the first insulating film 37, the etching process is suppressed from acting on the element isolation region 12b even if the formation position of the contact hole 39b extends over the element isolation region 12b because of the misalignment of the mask, for example.

After the first contact hole 39b is formed in the inter-level insulating film 38, as shown in FIG. 9B, an etchant used for the RIE (Reactive Ion Etching) process is changed to an etchant which easily etches the first insulating film 37 and is difficult to etch the element isolation region 12b. Then, the first insulating film 37 is etched to form a second contact hole 39b' in the first insulating film 37. As a result, the contact holes 39b, 39b' reaching the drain diffusion layer 21b, for example, are formed in the inter-level insulating film 38.

With the above contact forming method, the etching process is suppressed from acting on the element isolation region 12b even if the formation position of

the contact hole 39b extends over the element isolation region 12b. Therefore, it is prevented that the element isolation region 12b is etched and a hole exceeding over the pn junction between the diffusion layer 21b and the substrate 11 is formed. If the above hole is formed, for example, the bit line BL extends over the diffusion layer 21b and is brought into contact with the substrate 11. As a result, a junction leak will increase.

However, in the EEPROM according to this invention, the etching process can be suppressed from acting on the element isolation region 12b even if the formation position of the contact hole 39b extends over the element isolation region 12b. Therefore, an advantage that an increase in the junction leak can be suppressed can be attained.

The contact hole 39b may have a diameter larger than the width of the element region as shown in FIGS. 10A and 10B. In this case, the contact hole 29b overlaps the element isolation region 12b.

Thus, an increase in the junction leak can be suppressed in the EEPROM having the first insulating film 37 in the memory cell region 12. It is therefore preferable to leave the first insulating film 37 on that part of the diffusion layer in which a contact hole is to be made and a nearby part of the diffusion layer, while any other part of the film 37 is removed

after the annealing is effected in the oxidation atmosphere. FIG. 11 is a plan view of an EERROM of this type, which is the fourth embodiment of the invention.

(Fifth Modification of First Embodiment)

FIG. 12 is a cross sectional view showing a fifth modification of the NAND type EEPROM according to the first embodiment of this invention.

In the first embodiment, the first insulating film 37 is formed on the post-oxidation film 36, but this is not limitative. For example, as shown in FIG. 12, a second insulating film 51 such as a silicon dioxide film (which is also called a TEOS film) which permits an oxidizing agent to pass therethrough and is formed by using material gas of TEOS (Tetra Epoxy Silane) may be formed between the post-oxidation film 36 and the first insulating film 37.

In this case, for example, since the second insulating film 51 functions as a stopper when the first insulating film 37 is removed, the process margin can be enlarged.

(Second Embodiment)

In a case where a silicon nitride film is used as a first insulating film 37, there occurs a possibility that the reliability of the tunnel oxide film of a memory cell will be lowered since the silicon nitride film contains a relatively large amount of hydrogen and

it has relatively large mechanical film stress.

In this case, hydrogen can be extracted from the silicon nitride film and the film quality can be improved by subjecting the structure to the annealing process after deposition of the silicon nitride film in the oxidation atmosphere. Therefore, the effect for suppressing a lowering in the reliability of the tunnel oxide film of the memory cell can be sufficiently expected.

FIG. 13 is a cross sectional view showing a NAND type EEPROM according to a second embodiment of this invention. Further, FIGS. 14A, 14B, 14C, 14D are cross sectional views showing the NAND type EEPROM of the second embodiment of this invention in the respective main manufacturing steps.

The second embodiment will be explained together with the manufacturing method thereof.

First, as shown in FIG. 14A, a silicon substrate 11 (or well region) is subjected to the thermal oxidation process to form a gate oxide film (tunnel oxide film) 31 by the same method as that explained with reference to FIG. 5A. Then, gate electrodes 35 of stacked gate structure are formed on the gate oxide film 31 in a memory cell region 12 and gate electrodes 41 of single-gate structure are formed on the gate oxide film 31 in a peripheral circuit region 13. After this, the surfaces of the gate electrodes 35, 41 are

subjected to the oxidation process. The oxidation process is effected to compensate for the processing damage of the gate electrodes 35, 41, and as the result of the oxidation process, post-oxidation films 36 are formed on the surfaces of the gate electrodes 35, 41. Next, impurity 21' is ion-implanted into the silicon substrate 11 (or well region) with the gate electrodes 35, 41 and the element isolation region 12b used as a mask.

As shown in FIG. 14B, a silicon nitride film 37 is deposited on the structure shown in FIG. 14A by the same method as explained with reference to FIG. 5B. It is desired that the silicon nitride film 37 have a thickness of 50 nm or less.

Then, as shown in FIG. 14C, the doped impurity 21' is activated by effecting the annealing process in an oxidation atmosphere. In this case, the silicon nitride film 37 is subjected to the oxidation process to form a surface oxide film 37'. The surface oxide film 37' is so formed as to have a thickness of, for example, 1 nm to 10 nm. It is desired that the surface region of the silicon nitride film 37 be oxidized by strong oxidation, such as pyrogenic oxidation, water-vapor oxygen oxidation, ozone oxidation or oxygen-radical oxidiation. This is because strong oxidation can efficiently extract hydrogen from the silicon nitride film 37.

The silicon nitride film 37 on which the surface oxide film 37' is formed has a concentration gradient in which the hydrogen concentration gradually becomes higher from the surface side.

Thus, an influence by the hydrogen in the silicon nitride film 37 on the gate oxide film (tunnel oxide film) 31 is reduced and then the impurity 21' is laterally diffused towards portions below the gate electrodes 35, 41.

As a result, as shown in FIG. 14D, diffusion layers 21, 21a, 21b, 42, 43 are formed.

Next, after an inter-level insulating film 38 is formed on the structure shown in FIG. 14D, contacts 44 and interconnection layers 45 connected to the gate electrodes 41 are formed, contacts 39b and bit lines 40 connected to the drain diffusion layers 21b are formed, and contacts 39a and source lines connected to the source diffusion layers 21a are formed. Thus, a NAND type EEPROM with the construction shown in FIG. 12 is completed.

For example, as shown in FIG. 15, the hydrogen concentration of the silicon nitride film can be lowered and an electron trap amount dVg in the gate oxide film (tunnel oxide film) 31 can be reduced by forcedly forming the surface oxide film 37' on the surface of the silicon nitride film 37.

That is, if the surface of the silicon nitride

film 37 is subjected to the oxidation process before deposition of the inter-level insulating film 38, the hydrogen concentration of the silicon nitride film 37 can be lowered and the hydrogen concentration of the thermal oxide film 31 can be lowered. As a result, the electron trap amount dVg in the gate oxide film (tunnel oxide film) 31 can be reduced and the reliability of the tunnel oxide film can be prevented from being lowered.

The hydrogen concentration of the thermal oxide film shown in FIG. 15 is expressed by a relative value when it is set at "1" when the surface oxide film 37' is not formed.

Further, for example, the electron trap amount dVg is a difference between the maximum value and minimum value of the gate voltage occurring in a period 20 seconds when a negative voltage is applied to the gate and a D.C. constant current of approx. 0.1 A/cm^2 is caused to flow in the tunnel oxide film for approx. 20 seconds. In this case, the value of dVg becomes larger as the generation amount of electron trap in the tunnel oxide film becomes larger.

With the above construction, the reliability of the gate oxide film (tunnel oxide film) 31 can be suppressed or prevented from being lowered even if the silicon nitride film 37 is left behind on the memory cell region 12.

In the second embodiment, the silicon nitride film 37 is left behind on the peripheral circuit region 13, and it is possible to leave the silicon nitride film at least on the memory cell region 12 as in the first embodiment. In this case, in addition to the effect that the hydrogen concentration of the silicon nitride film 37 can be lowered, an advantage that the overlap amount or the like of the diffusion layer can be made different in the peripheral transistor and in the cell transistor can be attained.

In the second embodiment, the impurity 21' is doped into the substrate 11 before the silicon nitride film 37 is formed, but this is not limitative. For example, it is possible to dope the impurity 21' into the substrate 11 after the silicon nitride film 37 is formed.

The silicon nitride film 37 is not always necessary after the annealing process is effected in the oxidation atmosphere. Therefore, it is possible to remove all of the silicon nitride film 37 after the annealing process.

Further, this invention is not limited to the NAND type EEPROM and can be applied to an EEPROM other than the NAND type EEPROM, for example, an AND type EEPROM shown in FIG. 16A, NOR type EEPROM shown in FIG. 16B.

In the first and second embodiments, the post-oxidation film 36 is provided on the upper surface of

the control gate electrode 34 of stacked gate structure or on the upper surface of the gate electrode 41 of single-gate structure. Nonetheless, the control gates 34 and 41 may each comprise a conductive strip and either a silicon oxide film or silicon nitride film, which is provided on the conductive strip. In this case, the post-oxidation film 36 is provided on only the sides of the control gate electrode 34 or only the sides of the gate electrode 41.

In addition, this invention can be variously modified without departing from the technical scope thereof.

Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details and representative embodiments shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.

WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory device comprising:

a semiconductor substrate;

a first transistor formed in a peripheral circuit portion of the semiconductor substrate, a gate electrode of the first transistor having a first gate length;

a second transistor formed in a memory cell portion of the semiconductor substrate, a gate electrode of the second transistor having a second gate length shorter than the first gate length; and

a first insulating film formed above at least the memory cell portion, the first insulating film covering the second transistor and having a property which makes it difficult for an oxidizing agent to pass therethrough.

2. The nonvolatile semiconductor memory device according to claim 1, wherein the gate electrode of the second transistor has a stacked gate structure which includes a floating gate formed on a gate insulating film, an inter-gate insulating film formed on the floating gate and a control gate formed on the inter-gate insulating film.

3. The nonvolatile semiconductor memory device according to claim 1, further comprising:

a second insulating film which is different from

the first insulating film and formed between at least the second transistors and the first insulating film.

4. The nonvolatile semiconductor memory device according to claim 1, wherein the first insulating film is used as an etching stopper when contact holes are formed.

5. The nonvolatile semiconductor memory device according to claim 1, wherein the surfaces of the gate electrodes of the first and second transistors are oxidized.

6. A method for manufacturing a nonvolatile semiconductor memory device comprising:

forming a first gate electrode, which has a first gate length, on a peripheral circuit portion of a semiconductor substrate and a second gate electrode, which has a second gate length shorter than the first gate length, on a memory cell portion of the semiconductor substrate;

introducing impurity into the peripheral circuit portion and memory cell portion with at least the first and second gate electrodes used as a mask;

forming a first insulating film above at least the memory cell portion, the first insulating film covering the second transistors and having a property which makes it difficult for an oxidizing agent to pass therethrough; and

annealing the semiconductor substrate into which

the impurity has been introduced in an oxidation atmosphere to diffuse the impurity into the semiconductor substrate, whereby a first transistor having the first gate electrode and source and drain diffusion layers containing the diffused impurity is formed in the peripheral circuit portion and a second transistor having the second gate electrode and source and drain diffusion layers containing the diffused impurity is formed in the memory cell portion.

7. The method for manufacturing the nonvolatile semiconductor memory device according to claim 6, wherein at least the second gate electrode is formed by a method including steps of forming a gate insulating film on the semiconductor substrate, forming a floating gate on the gate insulating film, forming an inter-gate insulating film on the floating gate and forming a control gate on the inter-gate insulating film.

8. The method for manufacturing the nonvolatile semiconductor memory device according to claim 6, further comprising:

forming a second insulating film which is different from the first insulating film and formed between at least the second transistors and the first insulating film.

9. The method for manufacturing the nonvolatile semiconductor memory device according to claim 6, further comprising:

forming an inter-level insulating film above the semiconductor substrate after annealing the semiconductor substrate;

forming a first contact hole reaching the first insulating film in the inter-level insulating film; and

etching a part of the first insulating film which are exposed to the bottoms of the first contact hole and forming a second contact hole reaching a source/drain diffusion region of the second transistor in the first insulating film.

10. The method for manufacturing the nonvolatile semiconductor memory device according to claim 6, further comprising;

subjecting the surfaces of the first and second gate electrodes to an oxidation process.

11. A nonvolatile semiconductor memory device comprising:

a semiconductor substrate;

a transistor formed in a memory cell portion of the semiconductor substrate; and

a silicon nitride film whose surface is oxidized, the silicon nitride film covers the transistor.

12. The nonvolatile semiconductor memory device according to claim 11, wherein the silicon nitride film has a thickness of at most 50 nm.

13. The nonvolatile semiconductor memory device according to claim 11, wherein the thickness of an

oxide film on the surface of the silicon nitride film is not smaller than 1 nm and not larger than 10 nm.

14. The nonvolatile semiconductor memory device according to claim 11, wherein the concentration of hydrogen in the silicon nitride film is not larger than 3×10^{21} atom/cm^3.

15. A method for manufacturing a nonvolatile semiconductor memory device:

forming a transistor in a memory cell portion of a semiconductor substrate;

covering the transistor with a silicon nitride film; and

subjecting the surface of the silicon nitride film to an oxidation process.

16. The method for manufacturing the nonvolatile semiconductor memory device according to claim 15, further comprising:

forming an inter-level insulating film on the semiconductor substrate after subjecting the surface of the silicon nitride film to an oxidation process.

17. The method for manufacturing the nonvolatile semiconductor memory device, according to claim 15, wherein the surface of the silicon nitride film is oxidized by a method selected from the group consisting of pyrogenic oxidation and water-vapor oxygen oxidation.

18. The method for manufacturing the nonvolatile semiconductor memory device, according to claim 16,

wherein the surface of the silicon nitride film is oxidized by a method selected from the group consisting of pyrogenic oxidation and water-vapor oxygen oxidation.

ABSTRACT OF THE DISCLOSURE

A nonvolatile semiconductor memory device having a memory cell portion and peripheral circuit portion is disclosed. The nonvolatile semiconductor memory device has peripheral transistors formed in the peripheral circuit portion of a silicon substrate and cell transistors formed in the memory cell portion of the silicon substrate. The gate length of the cell transistor is shorter than the gate length of the peripheral transistor. Further, the nonvolatile semiconductor memory device has a silicon nitride film selectively formed on the memory cell portion. The silicon nitride film covers the cell transistors.

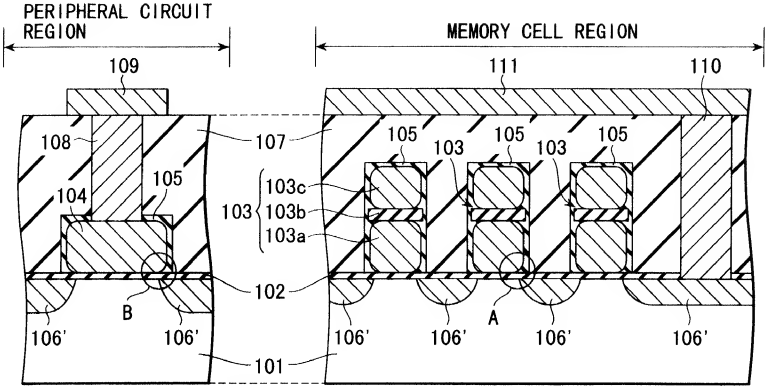


FIG. 1
PRIOR ART

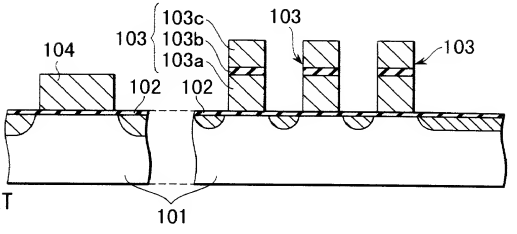


FIG. 2A
PRIOR ART

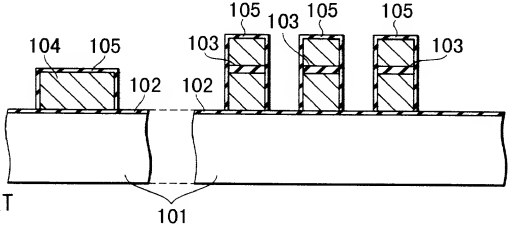


FIG. 2B
PRIOR ART

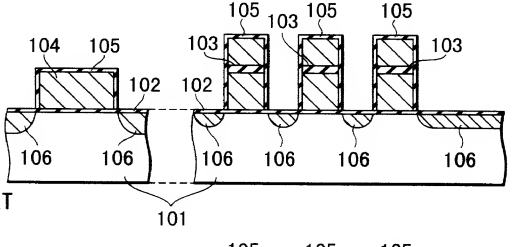


FIG. 2C
PRIOR ART

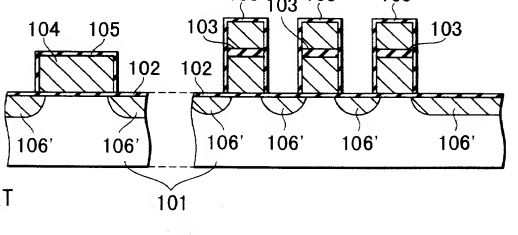


FIG. 2D
PRIOR ART

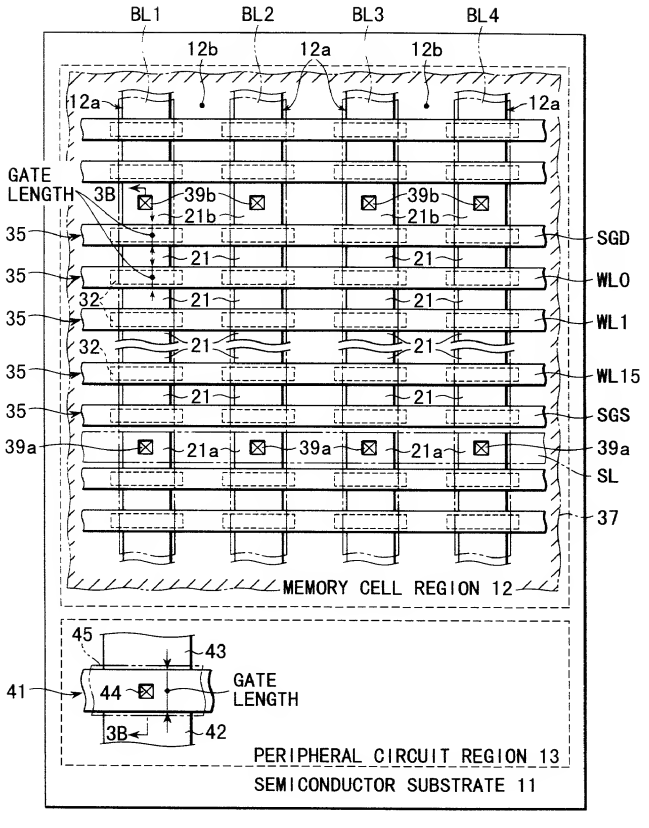

BL1
BL2
BL3
BL4
12b
12a
12b
12a
12a
GATE LENGTH
3B
39b
21b
39b
21b
35
35
35
35
35
35
32
32
21
21
21
21
21
21
21
21
SGD
WL0
WL1
WL15
SGS
39a
21a
39a
21a
39a
SL
37
MEMORY CELL REGION 12
45
43
41
44
GATE LENGTH
3B
42
PERIPHERAL CIRCUIT REGION 13
SEMICONDUCTOR SUBSTRATE 11

FIG. 3A

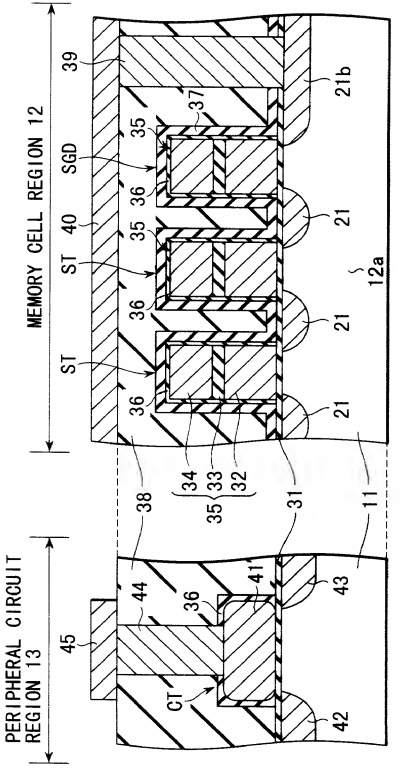


FIG. 3B

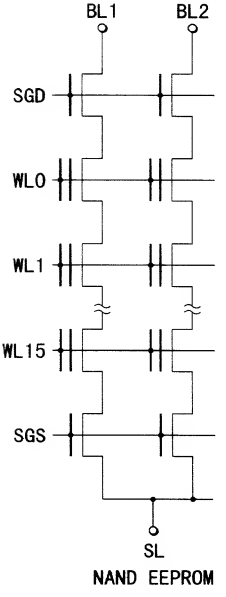


FIG. 4

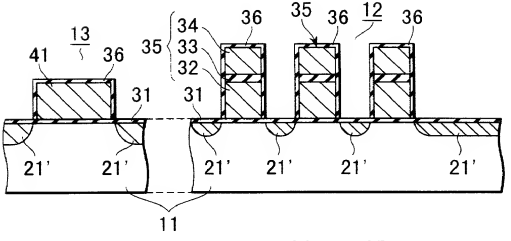


FIG. 5A

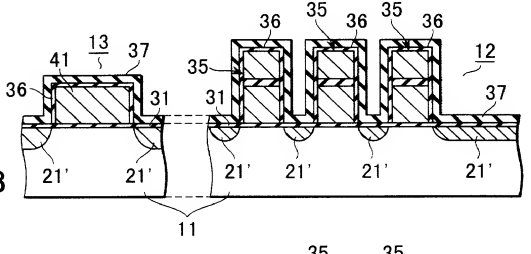


FIG. 5B

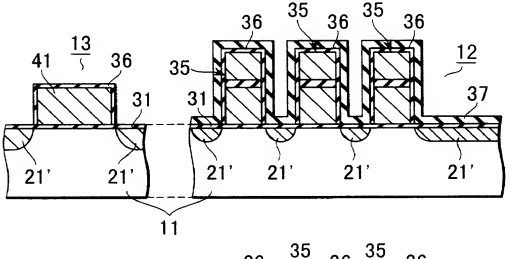


FIG. 5C

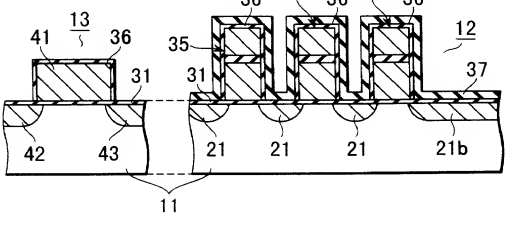


FIG. 5D

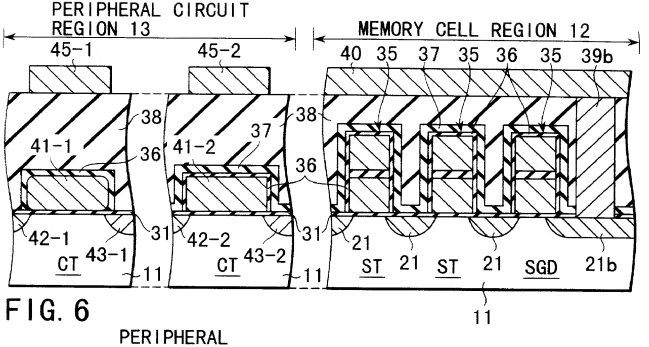


FIG. 6

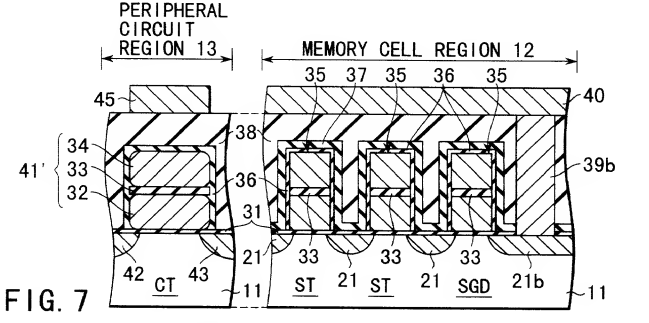


FIG. 7

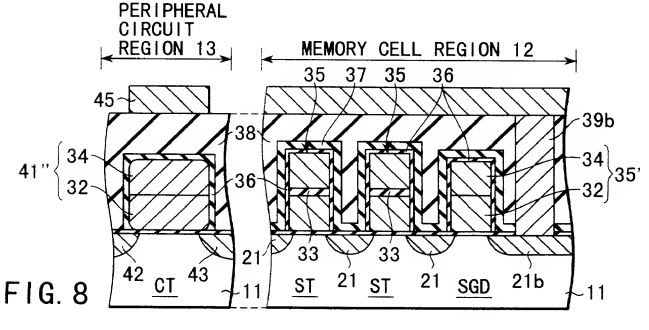


FIG. 8

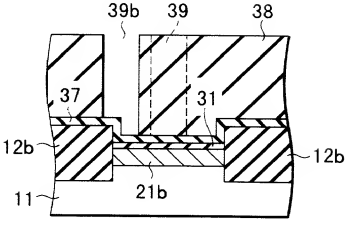


FIG. 9A

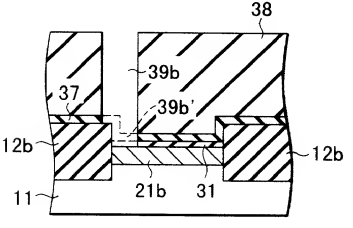


FIG. 9B

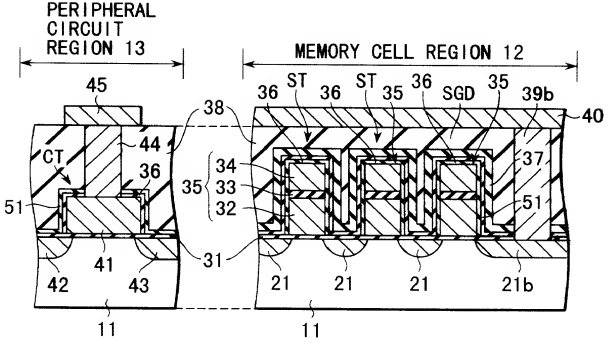


FIG. 12

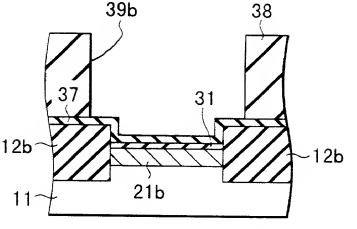


FIG. 10A

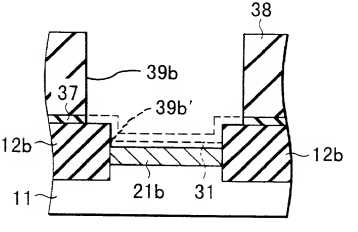


FIG. 10B

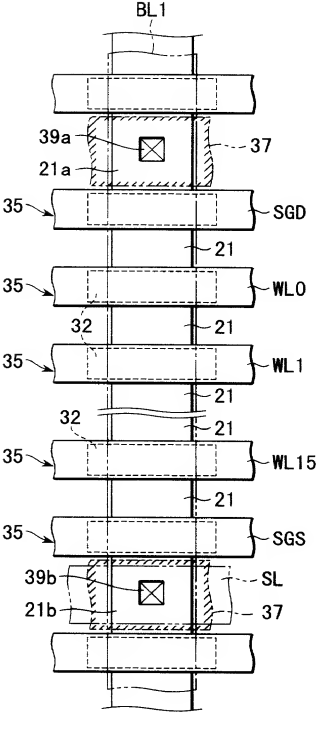

BL1
39a
37
21a
35
SGD
21
35
WL0
32
21
35
WL1
21
32
21
35
WL15
21
35
SGS
39b
SL
21b
37

FIG. 11

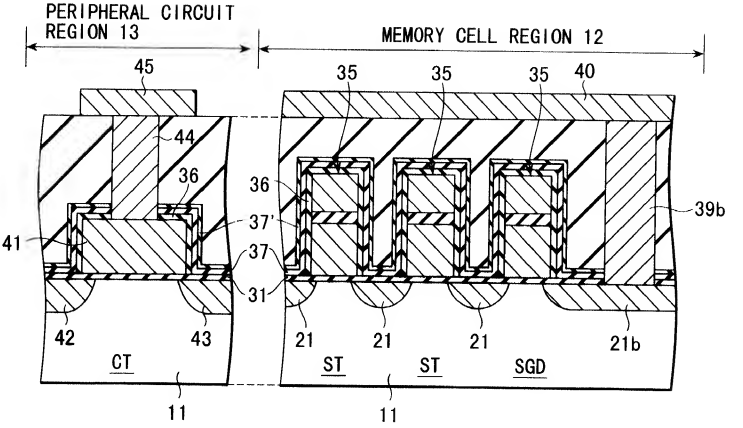


FIG. 13

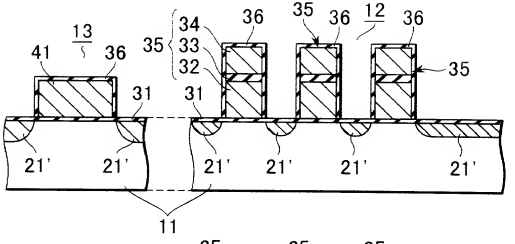


FIG. 14A

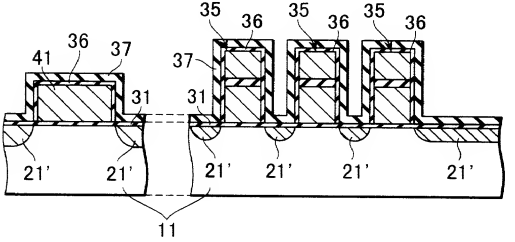


FIG. 14B

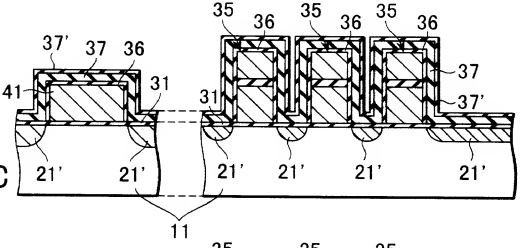


FIG. 14C

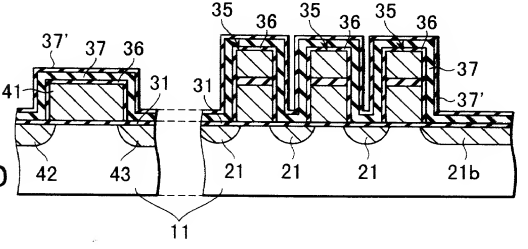
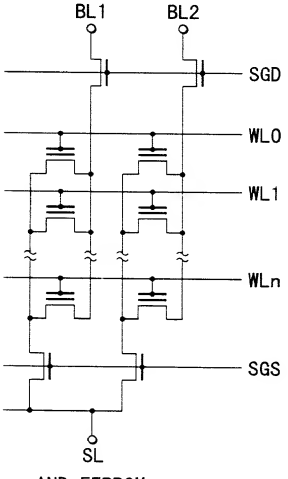


FIG. 14D

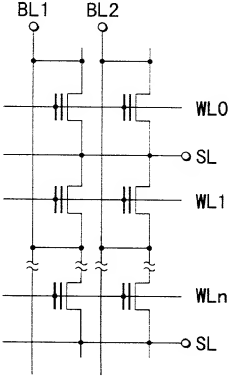
	CONCENTRATION OF HYDROGEN IN SiN FILM	CONCENTRATION OF HYDROGEN IN TUNNEL OXIDE FILM	dVg (ELECTRON AMOUNT TRAP)
NO SURFACE OXIDE FILM	4.0×10^{21} atom/cm^3	1	512mV
SURFACE OXIDE FILM FORMED	1.6×10^{21} atom/cm^3	0.2	398mV

FIG. 15



AND EEPROM

FIG. 16A



NOR EEPROM

FIG. 16B

Docket No. 0039-7692-2S

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Akira GODA, et al.

FILING DATE: Herewith

FOR: NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING THE SAME

LIST OF INVENTORS' NAMES AND ADDRESSES

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Listed below are the names and addresses of the inventors for the above-identified patent application.

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Kazuhiro SHIMIZU	Yokohama-shi, Japan
Hiroaki HAZAMA	Hachioji-shi, Japan
Hirohisa IIZUKA	Yokohama-shi, Japan
Seiichi ARITOME	Yokohama-shi, Japan
Wakako MORIYAMA	Yokohama-shi, Japan

A declaration containing all the necessary information will be submitted at a later date.

Respectfully Submitted,

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